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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,005	12/12/2000	Kazuyuki Ito	NEC 444	3384

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,005	ITO, KAZUYUKI	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election traverse of group I, claims 12-23 drawn to a method of making semiconductor device in Paper No. 5 is acknowledged.

Specification

2. The disclosure is objected to because of the following informalities:

page 7, lines 23 and 24 the sentence " a silicon nitride layer 2 is deposited on the silicon nitride layer 3" is not consistent with figure 8A. Appropriate correction is required.

Claim Objections

3. Claim 15 is objected to because of the following informalities: the limitation " reduction of said dummy" is not clear what it is referring. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 12, is rejected under 35 U.S.C. 102(e) as being anticipated by Bothra US patent No. 6,010,939.

Regarding claim 12, Bothra teaches a method for manufacturing a semiconductor device comprising the steps of: forming a shallow trench isolation layer

206 in a semiconductor substrate 200, so that active areas 204 and a field area including dummy areas DA (dummy active) for isolating the active areas and forming gates 216 on the active areas and dummy gates 226 on the dummy areas (fig. 2B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 13, is rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra in view of Nitta et al. US patent No. 6,225,230.

Regarding claim 13, Bothra teaches substantially the entire claimed process above except specifically detailing the process step involved in making the shallow trench isolation. Nitta teaches forming a first resist layer 110 with a predetermined pattern. An element isolation trench 115 is formed in the substrate 100 using the patterned resist layer and etching process, burying insulating layer 120 in the trench and finally performing a chemical mechanical polishing process on the insulating layer. It would have been obvious to one of ordinary skill in the art to incorporate Nitta's process steps to form STI into Bothra in order to isolate the active region.

Claims 14-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bothra.

Regarding claims 14 and 15, Bothra teaches substantially the entire claimed process of claim 12 above except specifically detailing the process step involved in

Regarding claims 14 and 15, Bothra teaches substantially the entire claimed process of claim 12 above except specifically detailing the process step involved in making gates and dummy gates where the step involves forming a conductive layer on the semiconductor substrate, forming a second photoresist (PR) layer on the conductive layer where the PR pattern layer have a gate pattern corresponding to the active areas and the dummy gate pattern corresponds to the dummy gate and finally patterning the conductive layer by a photolithography and etching process using the second photomask and forming dummy gate pattern by reduction of the dummy area patterns. It is conventional to deposit a conductive layer on semiconductor substrate and patterning it and forming photoresist mask corresponding to gate structures dummy as wells as functional gate patterns using conventional photolithographic techniques. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate and the dummy gate structure of Bothra's using conventional patterning techniques as claimed above.

Regarding claims 16-19, Bothra teaches substantially the entire claimed process of claim 12 above except specifically stating that the dummy gates are square, rectangular, polygonal and circular. The shape of the dummy gates is a matter of design choice. It would have been obvious to one of ordinary skill to in the art at the time the invention was made to come up with the dummy gates shapes as claimed. In re Daily, 317 F.2d 699, 149 USPQ 47 (CCPA 1966).

Regarding claims 20-23, Bothra teaches substantially the entire claimed process of claim 12 above except stating that the dummy areas are arranged in rows and

columns and also the rows of the dummy areas are shifted from each other, columns of the dummy areas are shifted from each other and the rows and columns of the dummy areas are shifted from each other. The arrangement of the dummy areas is a matter of design choice. It would have been obvious to one of ordinary skill to in the art at the time the invention was made to arrange the dummy areas as claimed. In re Daily, 317 F.2d 699, 149 USPQ 47 (CCPA 1966).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-G are cited as being related to dummy gate on silicon substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
March 5, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800